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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,227	09/03/2003	Bin Yu	H1486	4868
45114	7590	09/23/2005	EXAMINER	
HARRITY & SNYDER, LLP 11240 WAPLES MILL ROAD SUITE 300 FAIRFAX, VA 22030			PRENTY, MARK V	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/653,227	Applicant(s) YU ET AL.	
	Examiner MARK PRENTY	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4,6,7,16,18 and 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,7,16,18 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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This Office Action is in response to the amendment filed on August 17, 2005.

Claims 16, 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by previously cited United States Patent 6,853,020 to Yu et al. (Yu).

With respect to independent claim 16, Yu discloses (see the entire patent, including the Figs. 1-7 disclosure) a semiconductor device comprising: an insulator 120; a semiconductor fin 210 formed on the insulator; a source region 220 connected to a first end of the fin and formed on the insulator; a drain region 230 connected to a second end of the fin and formed on the insulator; a first sidewall spacer 410 formed adjacent a first side of the fin in a roughly triangular shape; a second sidewall spacer 420 formed adjacent a second side of the fin in a roughly triangular shape; and a gate material layer 710 formed over the fin, the first sidewall spacer, and the second sidewall spacer, and in contact with the first and second sidewall spacers, in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material to smoothly transition over the fin and the first and second sidewall spacers, wherein the first and second sidewall spacers are formed to a width of about 150 Å to about 1000 Å (see column 4, lines 23-25).

Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yu.

With respect to dependent claim 18, Yu's first and second sidewall spacers 410 and 420 slope away from the fin 210.

Claim 18 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yu.

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With respect to dependent device claim 19, its recitation that the spacers "reduce micromasking effects during etching of a gate material to form the gate," does not structurally define over Yu's spacers 410 and 420.

Claim 19 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yu.

Claims 1-4, 6, 7, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over previously cited United States Patent Application Publication 2003/0151077 to Mathew et al. (Mathew) together with previously cited United States Patent 5,663,586 to Lin.

With respect to independent claim 1, Mathew discloses (see the entire publication, including the Figs. 12-16 disclosure) a semiconductor device comprising: an insulator 14; a semiconductor fin 18 formed on the insulator; a source region adjacent a first end of the fin formed on the insulator; a drain region adjacent a second end of the fin formed on the insulator; a first sidewall spacer 62' formed adjacent a first side of the fin, the first sidewall spacer having a substantially triangular shaped cross-section; a second sidewall spacer 64' formed adjacent a second side of the fin, the second sidewall spacer having a substantially triangular shaped cross-section; and a gate 66 formed over the fin and the first and second sidewall spacers, and in contact with the first and second sidewall spacers, in a channel region of the semiconductor device.

The difference, therefore, between claim 1 and Mathew is claim 1 recites that the sidewall spacers are formed with a width ranging from about 150 Å to about 1000 Å (Mathew does not disclose the width of its sidewall spacers).

Lin teaches that polysilicon sidewall spacers are conventionally formed with a width of about 200 Å to 1000 Å (see column 4, lines 39-46).

It would have been obvious to one skilled in this art to form Mathew's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick.

Claim 1 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 2, Mathew first and second spacers 62' and 64' cause a topology of the gate 66 to smoothly transition over the fin and the first and second sidewall spacers.

Claim 2 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 3, Mathew's first and second spacers 62' and 64' slope away from the fin.

Claim 3 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 4, Mathew's gate 66 includes an electrode portion formed away from the fin (see paragraph [0031], last sentence).

Claim 4 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 6, Mathew's first and second sidewall spacers 62' and 64' are formed of polysilicon (see paragraphs [0027-0028]).

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Claim 6 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 7, Mathew's gate 66 can comprise polysilicon (see paragraph [0029]).

Claim 7 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to independent claim 16, Mathew discloses (see the entire patent, including the Figs. 12-16 disclosure) a FinFET device comprising: an insulator 14; a semiconductor fin 18 formed on the insulator; a source region connected to a first end of the fin and formed on the insulator; a drain region connected to a second end of the fin and formed on the insulator; a first sidewall spacer 62' formed adjacent a first side of the fin in a roughly triangular shape; a second sidewall spacer 64' formed adjacent a second side of the fin in a roughly triangular shape; and a gate material layer 66 formed over the fin, the first sidewall spacer, and the second sidewall spacer, and in contact with the first and second sidewall spacers, in a direction perpendicular to a direction of the fin, whereby the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers.

The difference, therefore, between claim 16 and Mathew is claim 16 recites that the sidewall spacers are formed with a width of about 150 Å to about 1000 Å (An does not disclose the width of its sidewall spacers).

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Lin teaches that polysilicon sidewall spacers are conventionally formed with a width of about 200 Å to 1000 Å (see column 4, lines 39-46).

It would have been obvious to one skilled in this art to form Mathew's polysilicon sidewall spacers with a width of about 150 Å to about 1000 Å because Lin teaches that polysilicon sidewall spacers are conventionally formed that thick.

Claim 16 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent claim 18, Mathew's first and second sidewall spacers 62' and 64' slope away from the fin 18.

Claim 18 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

With respect to dependent device claim 19, its recitation that the spacers "reduce micromasking effects during etching of a gate material to form the gate," does not structurally define over Mathew's spacers 62' and 64'.

Claim 19 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew together with Lin.

The applicant's arguments with respect to the 35 U.S.C. 102(e) rejection based on Yu are persuasive with respect to independent claim 1 but not with respect to independent claim 16. Specifically, although Yu does not disclose claim 1's "a gate [structure] formed over the fin," Yu does disclose claim 16's "a gate material layer formed over the fin." See Yu's Fig. 7 disclosure, including the sentence bridging columns 4 and 5.

Furthermore, Yu does disclose to one skilled in the art that the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over the fin and the first and second sidewall spacers. In this regard, note newly cited United States Patent 4,807,013 to Manocha.

The applicant's arguments with respect to the 35 U.S.C. 103(a) rejection based on Mathew together with Lin are not persuasive.

First, the applicant's argument: "Mathew does not disclose 'a gate formed over the fin and the first and second sidewall spacers,' as is recited in claim 1," is incorrect. See Mathew's Fig. 14 and Fig. 16, which clearly disclose gate 66 formed over the fin 18 and the first and second sidewall spacers 62' and 64.

Furthermore, the applicant's argument that Mathew's and Lin's FET structures "would be recognized by one of ordinary skill in the art as different types of semiconductor FET structures and that specific parameters (such as the width of a spacer) in one device could not simply be applied to the other device," is incorrect. Specifically, Mathew and Lin are both directed to insulated gate field effect transistors (IGFETs) comprising gate sidewall spacers, so one of ordinary skill in the art would have been applied Lin's IGFET gate sidewall spacer width teaching to Mathew's IGFET gate sidewall spacer, particularly insofar as Mathew does not disclose the width of its IGFET gate sidewall spacer.

Finally, Mathew does disclose to one skilled in the art that the first and second sidewall spacers cause a topology of the gate material layer to smoothly transition over

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the fin and the first and second sidewall spacers. In this regard, note newly cited United States Patent 4,807,013 to Manocha.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.


Mark V. Prenty
Primary Examiner